

HC-DSV136N

RF power field effect transistor

1. Product profile

1.1 General description

A 15 W silicon RF-MOS power transistor for broadcast applications and industrial applications in the HF and VHF band. Designed primarily for wideband large-signal output to 400MHz.

Table 1. Production test information

Mode of operation	F (MHz)	VDD(V)	P _L (W)	G _p (dB)	η_D (%)
CW	150	28	27	21	78

1.2 Features

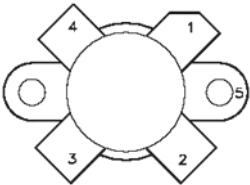
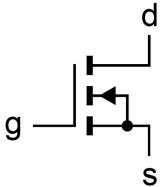
- ◆ Common source configuration
- ◆ Typical CW performance @ Freq=150MHz, V_{DD}= 28Vdc , I_{DQ}=100mA
Average output power = 25 W
Power gain = 21 dB
Efficiency = 78 %
- ◆ Excellent thermal stability
- ◆ Excellent ruggedness
- ◆ High power gain
- ◆ High efficiency
- ◆ 10:1 VSWR capability
- ◆ Easy power control

1.3 Applications

Industrial, scientific and medical applications
Broadcast transmitter applications

2 Pinning information

Table 2.Pinning

Pin	Description	Simplified outline	Graphic symbol
1	Drain		
3	Gate		
2、4、5	Source (Flange)		

3 Limiting values

Table 3.Limiting values

Symbol	Rating	Values	Unit
VDSS	drain-source voltage	90	V
VGS	gate-source voltage	±30	V
ID	drain current	5	A
Tstg	storage temperature	-65 to +150	°C
T _j	junction temperature	200	°C

4 Thermal characteristics

Table 4.Thermal characteristics

Symbol	Parameter	Typ.	Unit
Rth(j-c)	thermal resistance from junction to case	2.6	°C/W

5 Characteristics

Table 5. DC characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V(BR)DSS	drain-source breakdown voltage	V _{GS} = 0 V; I _D = 1 mA	75	-	-	V
VGS(th)	gate-source threshold voltage	V _{DS} = 10 V; I _D = 50 mA	1.0	2.7	5.0	V
IDSS	drain leakage current	V _{GS} = 0 V; V _{DS} = 28 V	-	-	10	uA

IGSS	gate leakage current	$V_{GS} = \pm 30 \text{ V}; V_{DS} = 0 \text{ V}$	-	-	± 1	μA
gfs	forward transconductance	$V_{DS} = 10 \text{ V}; I_D = 3 \text{ A}$	0.8	1.0	-	S
RDS(on)	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 3 \text{ A}$	-	-	1.1	Ω
C_{rss}	feedback capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 28 \text{ V}; f = 1 \text{ MHz}$	-	4	-	pF
Ciss	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 28 \text{ V}; f = 1 \text{ MHz}$	-	76	-	pF
Coss	output capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 28 \text{ V}; f = 1 \text{ MHz}$	-	36	-	pF

Table 6. RF characteristics

Mode of operation: CW; $f = 150 \text{ MHz}$; RF performance at $V_{DD} = 28 \text{ V}$; $I_{DQ} = 100 \text{ mA}$;
 $T_{case} = 25 \text{ }^\circ\text{C}$; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_L = 150 \text{ W}$	-	21	-	dB
η_D	drain efficiency	$V_{DS} = 28 \text{ V}$ $I_{DQ} = 100 \text{ mA}$	-	78	-	%
VSWR	Load Mismatch Tolerance	$f = 150 \text{ MHz}$	10:1	-	-	%

6. Ruggedness in class-AB operation

The DSV136N is capable of withstanding a load mismatch corresponding to VSWR = 10: 1 through all phases under the following conditions: $V_{DD} = 28 \text{ V}$; $I_{DQ} = 100 \text{ mA}$; $P_L = 150 \text{ W}$; $f = 150 \text{ MHz}$.

7. Test Circuit

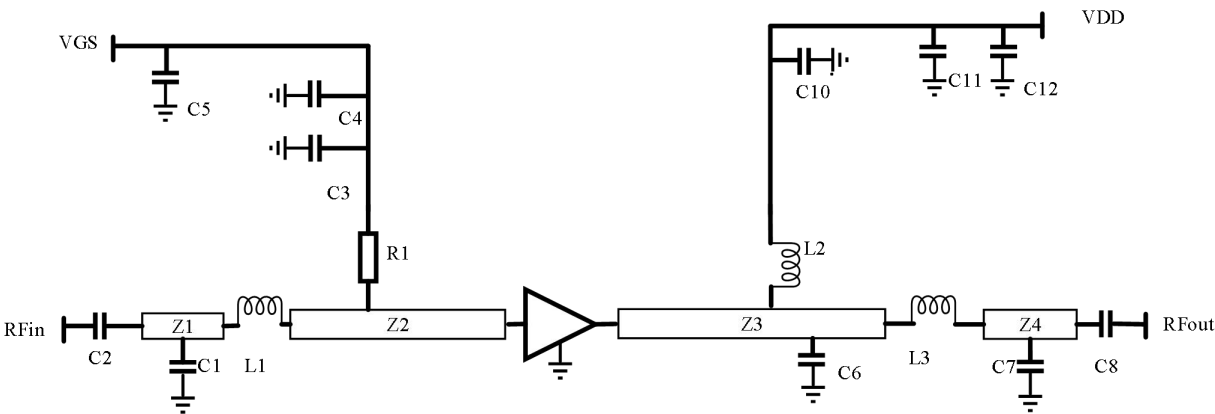


Fig 1. 150MHz Test Circuit

Table 7. List of components

All capacitors should be soldered vertically.

Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	39 pF	
C2, C8	multilayer ceramic chip capacitor	680 pF	
C3,C10	multilayer ceramic chip capacitor	1nF	
C4	multilayer ceramic chip capacitor	100pF	
C5	multilayer ceramic chip capacitor	10uF	
C6	multilayer ceramic chip capacitor	7.5pF	
C7	multilayer ceramic chip capacitor	24pF	
C9	multilayer ceramic chip capacitor	18 pF	
C11	multilayer ceramic chip capacitor	100nF	
C12	multilayer ceramic chip capacitor	10uF	Electrolytic capacitor
L1	Chip inductor	68nH	
L2	6 turns enameled copper wire	D = 0.5 mm; length = 105 mm	
L3	2 turns enameled copper wire	D = 0.5 mm; length = 10 mm	
R1	chip resistor	150Ohm	
Z1	Strip line		(L x W) 6.5mm×2.2mm
Z2	Strip line		(L x W) 9.4mm×2.2mm
Z3	Strip line		(L x W) 13.5mm×2.2mm
Z4	Strip line		(L x W) 6.1mm×1.9mm
Printed-Circuit Board (PCB):	Rogers 4350B; $\epsilon_r = 0.030$ " F/m; height = 1mm; Cu (top/bottom metallization);		

8. Test information

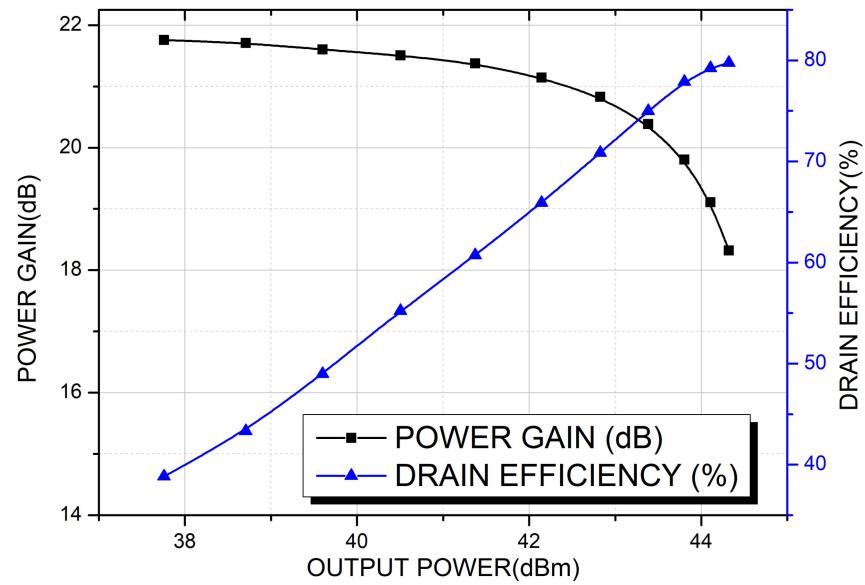


Fig 2. Power Gain and PAE versus Output Power @F=150MHz CW, $V_{DD}=28V$, $I_{DQ}=100mA$

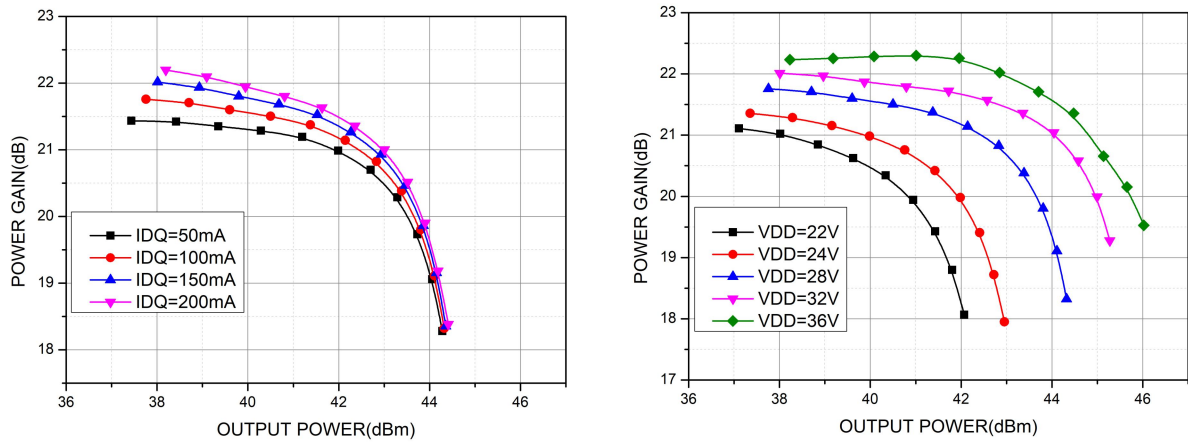
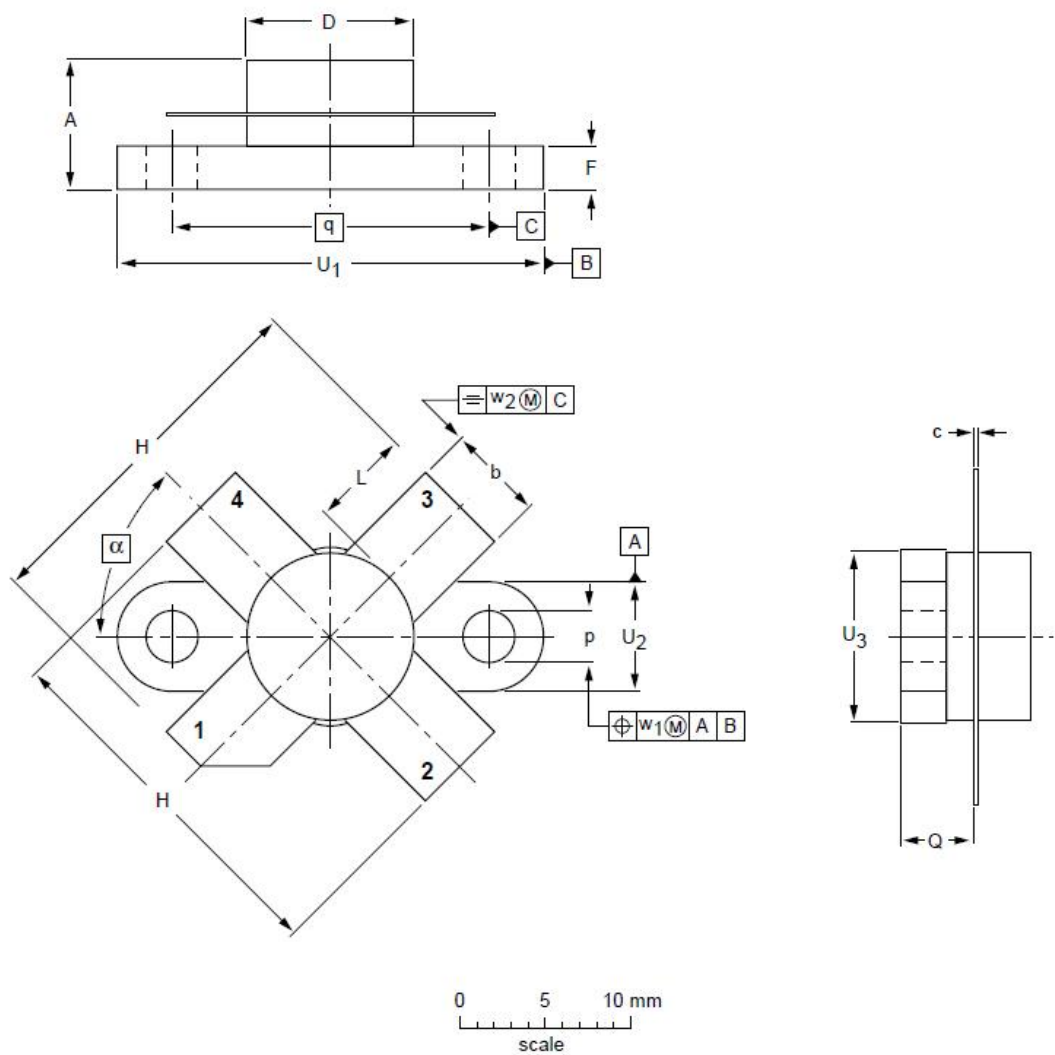


Fig 3. Power Gain versus Output Power

9. Package outline



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D ₁	F	H	L	p	Q	q	U ₁	U ₂	U ₃	w ₁	w ₂	α
mm	7.47 6.37	5.82 5.56	0.18 0.10	9.73 9.47	9.63 9.42	2.72 2.31	20.71 19.93	5.61 5.16	3.33 3.04	4.63 4.11	18.42	25.15 24.38	6.61 6.09	9.78 9.39	0.51	1.02	45°
inches	0.294 0.251	0.229 0.219	0.007 0.004	0.383 0.373	0.397 0.371	0.107 0.091	0.815 0.785	0.221 0.203	0.131 0.120	0.182 0.162	0.725	0.99 0.96	0.26 0.24	0.385 0.370	0.02	0.04	